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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/735,061
Filing Date: December 11, 2003
Appellant(s): LUK ET AL.

Nathaniel T. Wallace
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2 February 2009 appealing from the Office action mailed 20 February 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,757,693	Houghton et al.	5-1998
2003/0147277	Hsu	8-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1, 2, and 58** are rejected under 35 U.S.C. 102(b) as being anticipated by Houghton et al. (US 5,757,693) ("Houghton").

3. **Regarding claim 1,** Houghton discloses, in figure 1, a gated diode memory cell comprising: at least one transistor (for example Tw0) having a diffusion region and a gate connected directly to a write wordline (WLW0); and a gated diode (for example Tr0) having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline (for example WLR0).

4. **Regarding claim 2,** Houghton discloses, in figure 1, a gated diode memory cell as defined in Claim 1 wherein the first terminal of the gated diode (for example Tr0) forms one terminal of a storage cell and the second terminal of the gated diode (for example Tr0) forms another terminal of the storage cell.

5. **Regarding claim 58,** Houghton discloses, in figure 1, a gated diode memory cell as defined in claim 1 wherein the at least one transistor (for example Tw0) and gated diode (for example Tr0) are a same type of FET (see figure 1).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 3-10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Houghton et al. (US 5,757,693) ("Houghton") in view of Hsu (US 2003/0147277).

8. **Regarding claim 3,** Houghton discloses a gated diode memory cell as defined in claim 2 wherein the first terminal is a gate of the gated diode.

9. Houghton does not disclose wherein the gate is implemented in the form of a shallow trench.

10. Hsu discloses in figures 4 and 9A-9D a gated diode memory cell wherein the gate (906A) is implemented in the form of a shallow trench (abstract and [0064]).

11. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the device of Houghton with a gate that is implemented in the form of a shallow trench in view of the teachings of Hsu for the purpose of achieving significant area reduction ([0016] of Hsu).

12. **Regarding claim 4,** the Houghton/Hsu combination further discloses a gated diode memory cell as defined by claim 3, wherein the gate of the (for example 906A in figure 9D of Hsu) of the gated diode (for example 220 of Hsu) comprises a poly trench (906A in figure 9D of Hsu) surrounded by thin oxide (905B of Hsu) with silicon (for

example 913 of Hsu) disposed underneath and surrounding the thin oxide (905B of Hsu) (see also [0069] of Hsu).

13. **Regarding claim 5,** the Houghton/Hsu combination further discloses a gated diode memory cell as defined in Claim 4 wherein the poly trench (906A of Hsu) is cylindrical (see figures 9A-9D of Hsu).

14. **Regarding claim 6,** the Houghton/Hsu combination further discloses a gated diode memory cell as defined in claim 4 wherein the gate (for example 906A in figure 9D of Hsu) of the gated diode (for example 220 of Hsu) comprises a metal oxide semiconductor ("MOS") capacitor ([0064] and [0033] of Hsu).

15. **Regarding claim 7,** Houghton discloses a gated diode memory cell as defined in Claim 2.

16. Houghton does not disclose wherein the gate of the gated diode is planar.

17. Hsu discloses in figures 4 and 3A-3B wherein the gate (216) of the gated diode (for example 220) is planar (see figure 3A).

18. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the device of Houghton with a gate that is planar in view of the teachings of Hsu since planar gates are commonly used in the art.

19. **Regarding claim 8,** the Houghton/Hsu combination further discloses a gated diode memory cell as defined in Claim 7 wherein the gate (216 of Hsu) of the gated diode (for example 220 of Hsu) is disposed above a diffusion area (below 215 in figure 3A of Hsu).

20. **Regarding claim 9,** the Houghton/Hsu combination further discloses a gated diode memory cell as defined in Claim 8, further comprising an oxide layer (215 of Hsu) disposed between the gate (216 of Hsu) of the gated diode (220 of Hsu) and the diffusion area (below 215 of Hsu).

21. **Regarding claim 10,** the Houghton/Hsu combination further discloses a gated diode memory cell as defined in Claim 7, wherein the gated diode (220 of Hsu) comprises a planar metal oxide semiconductor ("MOS") capacitor([0033] of Hsu).

(10) Response to Argument

Examiner respectfully traverses Appellant's arguments regarding claim 1.

Appellant argues that Houghton fails to address the limitation "connected directly to the diffusion region of the at least one transistor" because the storage node SN0 intervenes between the transistor Tr0 and transistor Tw0 which precludes the claimed structure of a direct connection.

In response the gated diode Tr0 has a first terminal, i.e. the gate terminal, connected directly to the diffusion region of the transistor Tw0 precisely as shown and defined by the storage node SN0. A node is a representation of a direct connection. The storage node is not an intervening layer or device that would preclude a direct connection but rather a means by which the gate of the gated diode is directly connected to the diffusion region of the transistor Tw0.

Appellant argues that the transistor Tr0 cannot be the claimed "gated diode".

In response there is no structure claimed that structurally distinguishes the claimed "gated diode" from the transistor Tr0. "Gated diode" is merely a label since no

structure is claimed. Furthermore, transistor Tr0 can be interpreted to be a “gated diode”. A diode is a two terminal device. A transistor has the capability of functioning as a two terminal device depending on the voltage applied to the terminals. For example, by applying a common voltage to the gate and drain terminals thereby effectively connecting the gate to the drain, the transistor is a diode. Furthermore, field effect transistors comprise a gate and a diode. The junction between the source/drain region and the oppositely doped channel region is a p-n junction, i.e. a diode. Therefore, the transistor Tr0 is a "gated diode".

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner’s answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Allison P. Bernstein/

Allison P. Bernstein

29 April 2009

/Richard Elms/ 5.4.09

Supervisory Patent Examiner, Art Unit 2824

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TQAS TC 2800